Processing techniques for 3-D integration techniques

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Processing techniques that address the interconnect issues required for fabrication of deep sub-micron electronic devices and for three-dimensional (3-D) integration of these components will be described. As the interconnect density increases, alternate methods of providing input/output (I/O) leads on a chip are required. One attractive approach to providing increased connectivity is to use through-wafer interconnects. This reduces the interconnect density on the front surface while providing additional I/Os on the back surface. It also provides a convenient mechanism for integrating two or more die to form a 3-D integrated structure. Processing techniques under development include: high aspect ratio silicon etching, insulator lining, adhesion/barrier layer deposition, seed layer deposition, electroplating, and chemical mechanical planarization (CMP).
The primary challenge to implementing 3-D stacking is the formation of high aspect ratio interconnects with a sufficiently small diameter and, consequently, with sufficiently high density. The techniques used for fabrication of the vertical interconnects need to be compatible with CMOS technology and executed within the thermal budget of completed ICs.

Keywords: Interconnect; Through-wafer; High aspect ratio etching; Insulator lining; Adhesion/barrier deposition; Electroplating; Chemical mechanical planarization (CMP)

1. Introduction and motivation

In recent years it has been recognized that on-chip and off-chip interconnects, rather than the transistor, are the limiting factors that dominate the performance and cost of future electronic components in high-performance ICs [1]. This realization has led to research on three-dimensional (3-D) integration approaches that rely on vertical interconnects and stacked die [2]. The development of 3-D integration technologies is motivated by shorter chip-to-chip interconnects, reduced parasitic effects and, hence, faster signal processing and reduced power consumption, as compared with side-by-side chip placement or large die system-on-chip approaches.

Through-wafer vertical interconnects are considered to be a critical technology for 3-D stacking of electronic chips, which is believed to be a solution to the performance bottleneck associated with traditional, inherently long 2-D chip-to-chip interconnects. Due to small lead lengths offered by through-wafer interconnects, one can expect a dramatic increase in the overall device speed, and a decrease in power requirements, as well as a decrease in analog noise and cross-talk, especially elimination of optical obscuration problems in the case of optoelectronic devices. In addition to making 3-D stacking possible, through-wafer interconnects offer performance improvements for non-stacked, individual device die as well. The ability to form backside contact pads to integrated circuits (ICs) built on the front surface of the wafer opens new possibilities for flip chip technology. The traditional flip chip concept does not allow for interconnection of more than two chips. When combined with through-wafer interconnects, however, three chips can be joined, offering tremendously increased I/O counts. Further, using through-wafer interconnects offers the ability to bond one of the active chips to the backside of the other (as opposed to the face-to-face bonding in the conventional flip chip technology), a configuration essential for many optoelectronic devices in which the optical signal is sent or received from the front surface of the device. Further, vertical interconnects give the opportunity to bond an active device to a passive component layer, containing resistors, inductances, or power/ground planes.

As in the case of stacking, geometrical parameters of vias used for formation of through-wafer interconnects are application dependent. Ideally, the vias may need to be as small as the standard contact pad, which is about 30×30 μm in today's ULSI technology, but practical requirements may not be as stringent for some applications. For example, biosensor arrays will require vias with a diameter and density of about 100 μm and 10^2/cm^2, respectively. High-resolution MEMS optical mirror arrays will require through-wafer vias with a diameter of approximately 50 μm and density of the order of 10^4/cm^2. The aspect ratio of vias is determined by the thickness of the substrate. Four inches diameter silicon wafers can be thinned to about 300 μm without negatively impacting wafer handling during formation of the through-via vertical interconnects (TVIs). The primary obstacles to implementing the 3-D stacking concept and extensions of the flip chip concept have been: 1) the inability to form high aspect ratio interconnects with sufficiently small diameters and, consequently, with sufficiently high densities, and 2) the lack of techniques that are compatible with complementary metal-oxide semiconductor (CMOS) technology and can be executed within the thermal budget of completed ICs. Previous

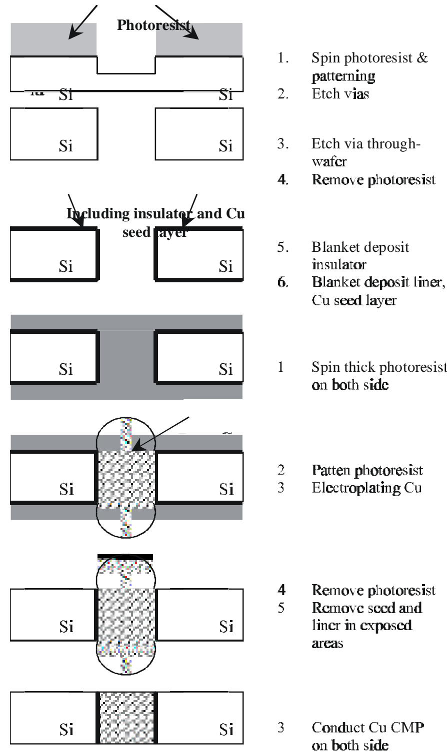

Figure 1. A schematic flow chart of the concept structure for through-wafer via vertical interconnects (TVIs).

efforts in the area of through-wafer via formation utilized either laser drilling [3,4] or wet etching process [5-7] in solutions of KOH or ethylenodiamine/pyrazine combinations. These etchants in (100) wafers lead to vias with sidewalls sloped at an angle of 54.7 deg with respect to the wafer surface. This limits the maximum aspect ratio (~0.7) and, consequently, the maximum packing density of these vias (~100/cm^2). In addition, due to the large area occupied by the interconnects, the capacitance of each via is too large for most applications. Further, KOH and similar etching agents are inherently not compatible with CMOS technology, and require the use of special fixtures sealing the wafer face against the etchants.

Historically, the simplest implementation of the 3-D integration concept has been to stack die without connecting them to each other. Sharp Microelectronics announced a three-die stacked memory device [8]. The size of the die decreases from the bottom to the top of the stack, and all three dies are wirebonded to the package. This approach simply saves space on the electronic circuit board.

A step further in 3-D integration is the use of metal traces on the side of the stack to form interconnects. This method has been developed by some companies such as Dense-PAC Microsystems and Irvine Sensors [9]. In addition to providing a means to stack die, the peripheral interconnect approach has the advantage of providing effective cooling to interconnects, but the number of I/O is limited.

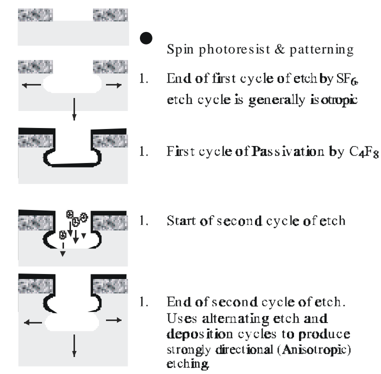

Figure 2. A schematic sketch of the Bosch etch process.

Development of interconnects on the side of the chip stack has also been an objective of recent work at the Korea Advanced Institute for Science and Technology. This version of the technology requires that the die be fabricated in a strip on a wafer [10]. The ultimate 3-D integration concept would use area array interconnects rather than the peripheral interconnects described above.

An earlier program reported in the literature was carried out in conjunction with the development of a massive parallel information processing system based on CMOS/SOS (silicon-on-sapphire) technology [11]. To form the interconnects, an array of vias was laser drilled through the wafer and a suitable conductor was formed using techniques such as capillary wetting, wedge extrusion, wire insertion, electroless plating, electroforming, or double-sided sputtering and electroplating. The main drawback of the laser drilling approach to forming the vias was the inherent limit on the diameter of via and the via density. Typically, the vias were about 60 μm in diameter and had a density of 1600/cm^2. Recent research at MIT has resulted in development of a high aspect ratio via in silicon to reduce ground inductance for RF and microwave circuits [12]. By similar etching, lining, and electroplating techniques, they demonstrate Faraday cages to isolate the system-on-a-chip (SOC) applications.

2. Experimental Approach

We are currently developing fabrication processes for high density, low capacitance through-wafer interconnects using a “Bosch” dry deep silicon etching process [13]. This process can be used to form deep vias with vertical sidewalls. The vertical or close-to-vertical sidewalls are an essential feature for formation of high density interconnects. The Bosch process has been more extensively used for formation of high aspect ratio MEMS structures, with typical feature sizes of the order of 100 μm, and needs, therefore, to be further developed and optimized for formation of high aspect ratio, small diameter, high density vertical interconnects. We anticipate new developments in controlling the profile of vias, the undercut beneath masking materials, and the uniformity of

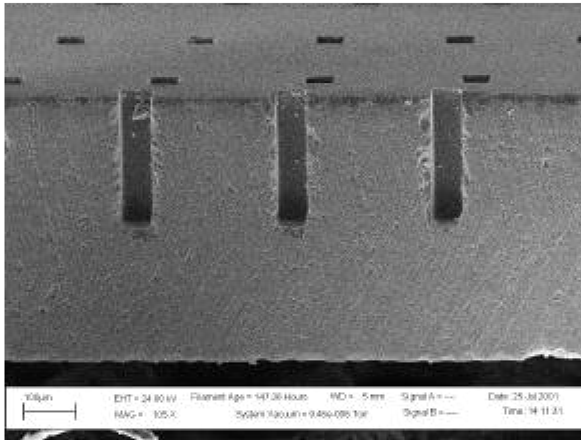

Figure 3. SEM micrograph of aspect ratio 5 vias etched by the Bosch etch process.

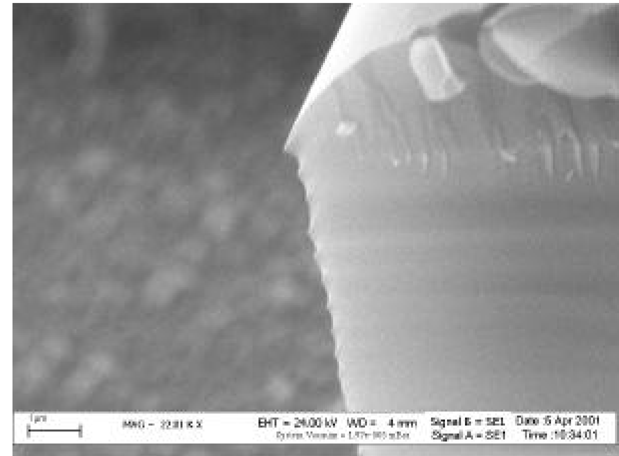

Figure 4. SEM micrograph of the scalloping resulting from the Bosch etch process.

geometrical parameters of vias across-wafer and wafer-to-wafer, as well as in controlling the potential damage to via sidewalls. The etching tool used in this project is an Oxford Instruments Plasmalab Model 100 system.

In order for the area array vertical interconnects to be formed, the etching of through-wafer vias needs to be followed by deposition of an insulating layer, deposition of a metal layer, and patterning of the metal layer to provide contacts to ICs and/or to form backside contact pads. The insulator and metal deposition need to result in films conformally deposited over the high aspect ratio features, and need to be conducted at temperatures compatible with the thermal budget of the completed IC and/or the thermal budget of the adhesives used in 3-D stacking, whichever is smaller.

Modified sputtering techniques and metal-organic chemical vapor deposition (MOCVD) techniques are under development for the formation of adhesion layer/diffusion barrier films and seed layers, followed by electroplating of copper to form the bulk of the metal interconnect. To insulate vias from one another, we are developing techniques for conformal deposition of an organic dielectric layer, parylene-C. A schematic flow chart is shown in Figure 1.

3. Summary of results

3.1 Through-wafer Via Etching

The Bosch process is used in the formation of vias, which are through-wafer with vertical sidewalls and have a high aspect ratio (approximately 10, greater than the aspect ratio of vias in ICs). The Bosch process is a series of etch and depositions cycles, each lasting only a few seconds. The deposition step coats the partially etched via with a protective polymer that prevents etching by radicals. In successive etch steps, the polymer coating on the bottom of the vias is removed by ion bombardment at the start of the etch cycle. Figure 2 shows a schematic illustration of the Bosch etch process. SF_6 and C_4F_8 are the gases used for etch and passivation, respectively. This process results in high selectivity to photo resist and etch rates in the range of 2-5 μm /min. The balance between etching and passivation is controlled by a wide variety of process parameters. Research studies have been performed to begin to understand the influence of process parameters, masking materials, and etch profiles of dry etched structures in silicon [14-16].

Figure 3 shows the vias of aspect ratio approximately 5 etched using the Bosch process. The overall etch rate for these vias was 1.8 μm /min. Table 1 shows the parameters used in this etch experiment. An additional advantage of the Bosch process is the ability to maintain an anisotropic

Table 1. The parameters used in the etch experiment utilizing the Bosch process for which the results are shown in figure 2.

	Plasma Power (13.56MHz, watt)		**Gas**		**Chamber Pressure** (mTorr)	**Time** (min.)	**Substrate Temperature** (^oC)
	Inductively	Bias	Type	Flow rates (sccm)			
Etching cycle	450	35	SF_6	85	30	15	0
Deposition cycle	450	15	C_4F_8	60	35	10	0

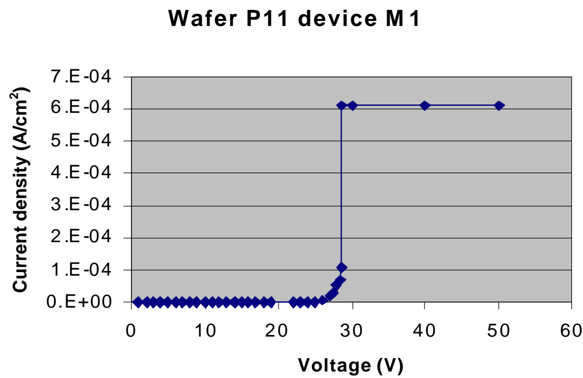

Figure 5. The electrical properties of a Parylene film.

profile, even if the etch portion of the process is isotropic. Use of an isotropic etch cycle allows one to maintain a high etch rates; the successive deposition step prevents lateral etching. If the etch is isotropic, there will be a small amount of undercut with each individual etch cycle. Since the process is cyclic, scalloping of the sidewall occurs as shown in Figure 4.

3.2 Lining/Metallization

In order to form vertical interconnects, etching of through-wafer vias is followed by deposition of an insulating layer, deposition of a metal layer, and patterning of the metal layer to provide contacts to ICs and/or to form backside contact pads. The insulator and metal deposition need to result in conformal thin film deposits over the high aspect ratio features at temperatures compatible with the thermal budget of the completed IC. Plasma enhanced CVD and/or organic vapor phase deposition is utilized to deposit an insulating layer on the sidewalls of the vias. RF magnetron sputtering is utilized to deposit a thin adhesion layer and metal-organic CVD (MOCVD) is utilized to deposit a conformal, continuous, and low resistivity seed layer.

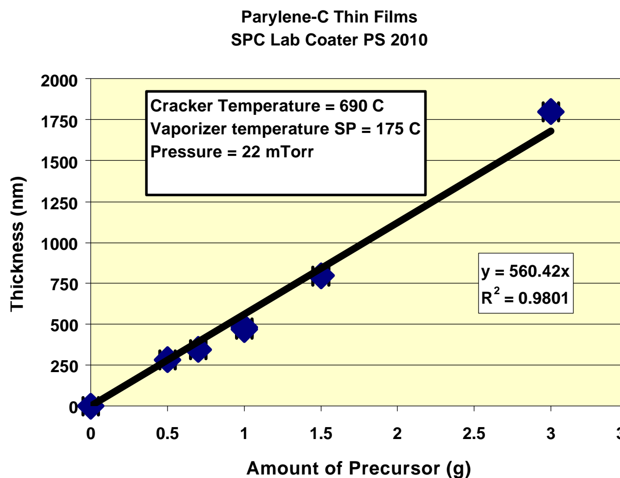

Figure 6. The thickness of a Parylene film plotted as a function of the amount of precursor. The variation run-to-run for a fixed amount of material was (3σ) =4%, and the thickness non-uniformality across a 4” wafer was (3σ) =5%.

Table 2. The candidate materials and deposition techniques for depositing the through-wafer via insulating layer.

Material	Deposition
Parylene-C	Vapor phase
SiN_x	PECVD
SiO_2	PECVD

Table 2 shows the candidate materials and deposition techniques for depositing an insulating layer on the through-wafer sidewalls of the vias. The materials in this table are listed in the order of decreasing risk and cost as well as compatibility, plus ease of process optimization. Parylene is a unique polymer series developed by Union Carbide Corporation. Detailed experimental results on the Parylene film are given below. Paralene was selected because it exhibits high conformability for high aspect ratio structures, low electrical leakage and high breakdown strength. Figure 5 shows the electrical properties of Parylene film. The dielectric constant (1mHz) is approximately 2.98, and the breakdown electric field is about 1.1 MV/cm for a 0.3 µm thick film. The file resistivity is approximately 10^{13} ohm-cm. Figure 6 shows the Parylene film thickness controlled by amount of precursor. Figure 7 demonstrates the excellent conformality of the Paralene layer, 48%, deposited over a high aspect trench formed in silicon.

PVD and CVD processes are techniques for depositing copper seed layer (metallization) after the process of deposition of the insulating layer. The PVD process has the advantage of a low process temperature and fair adhesion, but poor uniformity. On the other hand, the CVD process has moderate process temperature and good uniformity, but

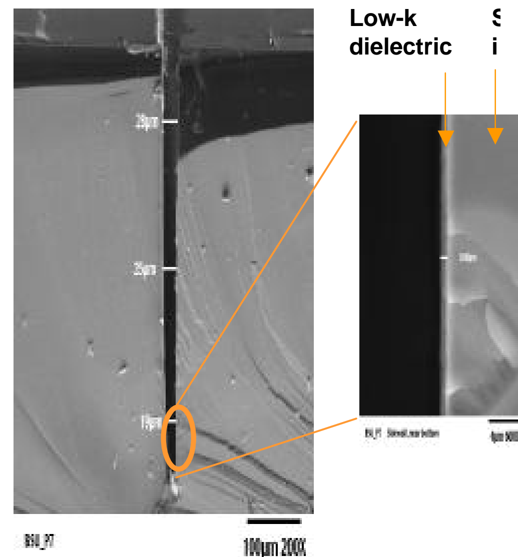

Figure 7. SEM micrograph of a thin Parylene layer deposited over a trench with an aspect ratio of 14; the conformality of the film was about 48%.

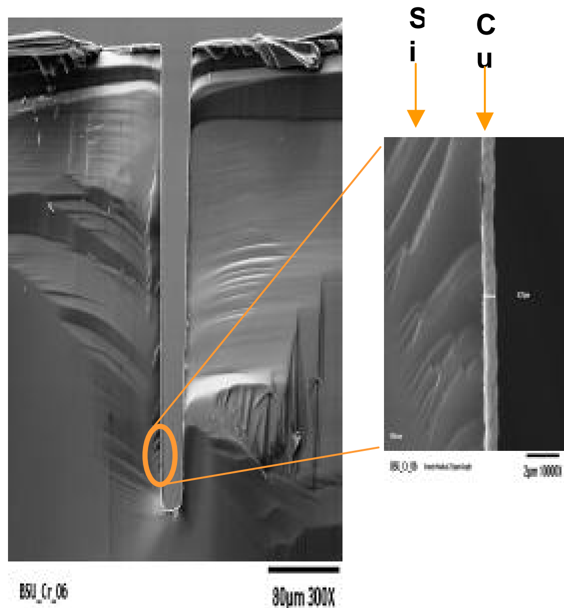

Figure 8. SEM micrograph of Cu seed layer deposited over a high aspect ratio trench; the comformality of the film was about 80%.

poor adhesion. Figure 8 demonstrates the conformality of the adhesion and copper seed layers deposited by MOCVD over a high aspect ratio trench. The conformality of the copper film is approximately 80%. Figure 9 shows the results of copper thickness as a function of depth by PVD and CVD processes, as deposited into 40 µm diameter silicon trenches.

3.3 Electroplating

Copper electrodeposition is being developed to provide the bulk of the metal interconnect. Copper electroplating is performed in a glass cell using a copper sulfamate plating solution. The electrical contact to the wafer is made through multiple metal fingers positioned along the wafer perimeter. This ensures a more uniform distribution of the electrical potential at the surface of the wafer than possible with a traditional single-point contact to the surface.

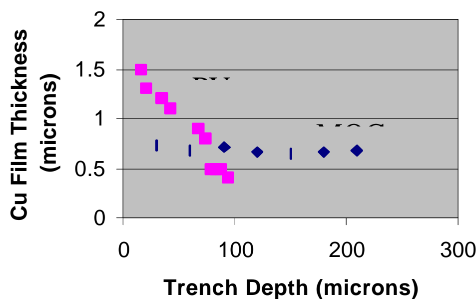

Figure 9. The copper thickness is shown as a function of depth for films deposited by PVD and CVD processes, as deposited into 40 µm diameter silicon trenches.

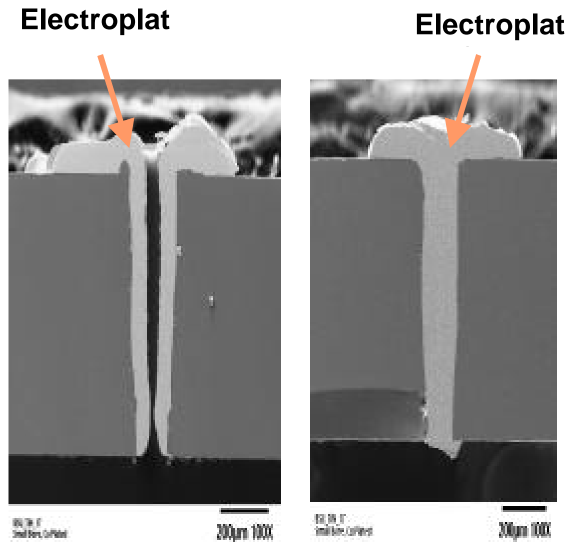

Figure 10. SEM micrographs of (a) partial and (b) full via filled by using electroplated copper on top of a MOCVD Cu seed layer.

Figures 10(a) and (b) present through-wafer vias coated with a sputtered TiN liner and a MOCVD Cu seed layer. They have been elelctroplated in the forms of either partial or full via fill, respectively.

3.4 CMP

Chemical mechanical planarization (CMP) will be developed on a Strasbaugh Model 6DS-SP polishing tool, to provide post-metal deposition planarization. The equipment consists of double rotating platens, wafer carrier, polishing pads, and slurry dispenser. The polishing is accomplished by the application of a copper polishing slurry to the wafer mounted on a rotating platen. An automated slurry feeding system ensures the uniform wetting of the polishing pad and the proper delivery and recovery of slurry. The microscopic action of polishing is both chemical and mechanical. The objective of this process is to planarize the wafer surface after via filling. Before the CMP process optimization could be addressed, a significant amount of time has been spent on developing a plan for the treatment of the Cu/slurry waste discharge [17].

4. Conclusions

Demonstration of through-wafer interconnects require development of many advanced processes. Anisotropic silicon etching for via formation and deposition of a conformal insulator lining in the via have been described and shown. Future development work will be performed in the areas of etching, lining/metallization, copper electroplating and copper CMP to allow an advanced interconnect technology that will be increasingly important in the integration of dissimilar processes and materials.

Acknowledgments

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