Charge trapping phenomenon in Al/SRO/Al on Si structure by lateral electrical stress

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In this article, the observation of charge trapping effect of silicon rich oxide (SRO) layer in an Al/SRO/Al on Si structure by lateral electrical stress is reported. The density of trapped charges depends on the deposition and post-treatment conditions of the SRO layer. For the Al/SRO/Al structure grown on n-Si substrates, positive trapped charges were observed. A model is proposed to interpret the experimental results.

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1. Introduction

The properties of silicon rich oxide (SRO) have been studied extensively due to the interesting characteristics of the photoluminescence and electrical conductivity as a function of excess silicon [1-4]. This material has several different potential applications, for example: active non-volatile memory devices, electron injection structures, optical and chemical sensors, light-emitting devices and probably in solar cells [5, 6, 7].

SRO films can be prepared by several techniques, such as chemical vapor deposition (CVD, thermal or plasma enhanced) and Si implantation into thermal silicon oxide grown on the crystalline Si substrate. When prepared by CVD, reactive gas mixture of N_2O and SiH_4 is usually used and the excess Si concentration can be controlled by the gas flow ratio $Ro=[N_2O]/[SiH_4]$. The excess Si concentration can be as high as 17% for Ro=3, and stoichiometric SiO_2 can be obtained for $Ro \geqq 50$ [3]. Infrared and ellipsometric studies have found that the as-deposited films present component of SiO_x ($x<2$), while thermal treatment at 1000°C or higher promotes the segregation of excess Si, resulting in the formation of the stoichiometric SiO_2 phase with Si nano-particles embedded [8]. Electrical investigation on this material has also found that, the transport of electrons in SRO is mainly via the direct tunneling through adjacent Si particles for the annealed films with high excess Si concentration [9].

It has been previously shown that very clear charge trapping effect can be obtained in the Al/SRO/Si MOS-like structure when applying a voltage between the gate electrode and back contact of substrate (vertical electrical stress) [10]. The trapped charges can be either positive or negative, depending on the bias of the gate voltage. This charge trapping effect depends on the properties of the SRO layer. For Ro ranging from 10 to 30, an enhancement of trapped charge density with increasing Ro is observed. Using this charge trapping effect, a new sensor structure has been proposed [7].

From the point of view of new device development, it would be very useful if the gate electrode, that reflects the incident light, could be removed, but keeping the charge-trapping effect. This could be possible only if one could charge the SRO layer without using a gate electrode. An alternative could be a lateral charge trapping. In this study, we report the experimental observation of the lateral charge trapping effect. A simple explanation for the experimental results is presented.

2. Experiments

Two kinds of samples were prepared: one is Al/SRO/Al on Si (called "single layer device") and another is Al/SRO/SiO_2/Al on Si (called "double layer device"). The Si substrates used are n-type (100) Si with resistivity of 3-9 Ohm-cm. A horizontal low pressure CVD hot-wall reactor using N_2O and SiH_4 as reactive gases was used for the deposition of SiO_2 and SRO layers. The deposition temperature was 700°C. For the deposition of SiO_2 layer, a gas flow ratio $Ro=[N_2O]/[SiH_4]=50$ was used. For the deposition of the SRO layer, two different Ro, 10 and 20, were used in order to produce different excess Si concentration in the SRO layer. The thicknesses of the SiO_2 and SRO layers are 350 Å and 800 Å, respectively. After the deposition, each sample was divided into two parts with one part being annealed at 1000°C/30 min in N_2 gas. On the SRO surface, Al gate electrodes were formed by standard photo-lithography technique. The electrode area is $1.4x10^{-2}$ cm^2. The back side of the Si substrate was implanted with phosphorus and aluminum was used to have a good contact. Finally, the samples were sintered at 450°C in forming gas for 20 minutes in order to get a good ohmic contact. In Table 1, the parameters of all samples used in this study are listed.

For the lateral electrical stress, we used a so-called "3-point configuration" as shown in Figure 1. The outside two electrodes (electrode 1 and 2) were used to apply the stressing voltage. In this case, the current will flow through the SRO layer and the underlying Si substrate laterally. The

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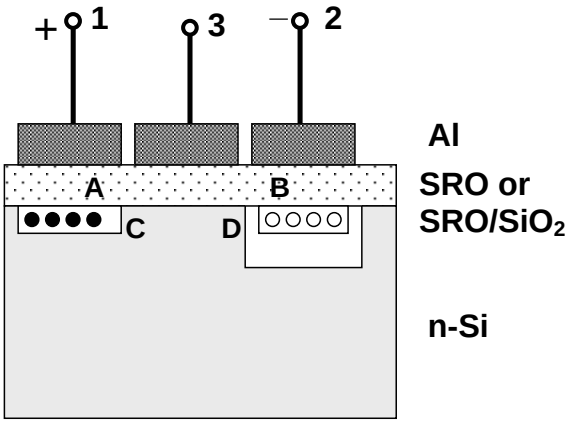
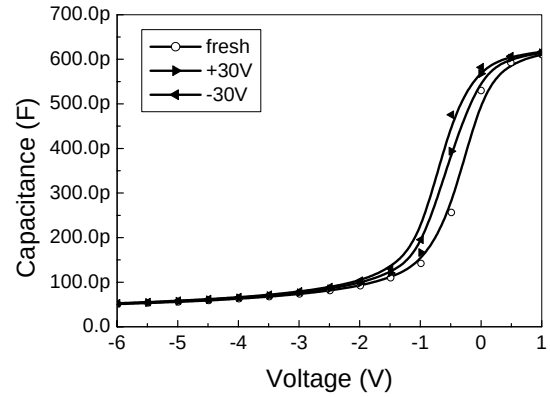


Figure 1. The "3-point configuration" used in the measurement. Electrodes 1 and 2 are used to apply the lateral stressing voltage; electrode 3 is used for the measurement of C-V curves. When a lateral electrical stressing voltage is applied, an accumulation layer is formed under electrode 1, wich is positively biased, while an inversion and depletion layers are formed under electrode 2 that is negatively biased. The stressing current can flow though both the SRO layer and the Si surface. The average potential of Si surface in region C-D is higher than that of SRO layer in region A-B.



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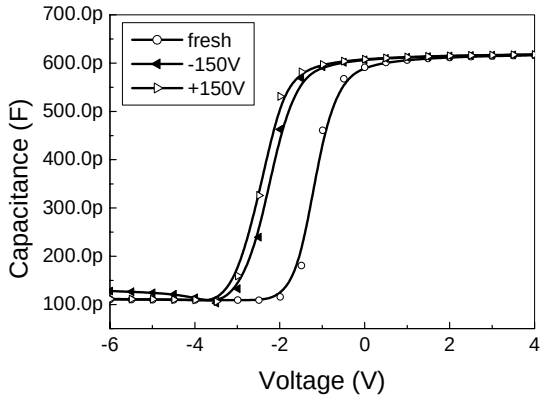


(b)

Figure 2: The CV curves of as-deposited Al/SRO/Al on Si devices before and after lateral electrical stress. (a) Ro=10 and (b) Ro=20.

middle electrode (electrode 3) was used to measure the charge trapping effect. The applied lateral stressing voltage ranges from 60V—120V. Capacitance vs. voltage characteristics (C-V) were measured in the middle electrode respect to the substrate before and after electrical stress was applied at different stressing times. The high frequency (100 kHz) C-V measurements were performed with a Keithley 590 C-V plotter computer controlled. All measurements were carried out in dark at room temperature.

3. Results

Figure 2 shows the C-V curves of the as-deposited single layer devices before and after lateral electrical stress (Sample N1 & N3). Both samples with Ro=10 and 20 show a clear shift in the C-V curves after the lateral electrical stress. The stress always moves the C-V curves to the left side (negative voltage side), being independent of the bias of stressing voltage. Another result demonstrated in this figure is that the shift for the sample with Ro=20 is larger than that of Ro=10.

Figure 3 shows the C-V curves of the annealed single layer devices before and after lateral stress (Sample N2 & N4). A clear shift to the left in C-V curves can be observed. However, the annealing treatment increases the shift for samples with Ro=10 and decreases the shift for sample with Ro=20, compared with the as-deposited corresponding samples.

Figure 4 and Figure 5 show the C-V curves of the as-deposited and annealed double layer devices before and after lateral electrical stress (Sample N7-N8). These figures show that no shift in C-V curves can be observed after lateral electrical stress when inserting an insulating SiO_2 layer between SRO and Si substrate.

4, Discussion

Early research has found that, there are two kinds of defect states in the interface region of SiO_2/Si [11]. The first kind is donor-like defects that are located just above the valence band edge. The donor-like defect is neutral when occupied by an electron and becomes positively charged when it loses an electron; the second kind is acceptor-like defects that are located just below the conduction band edge. The acceptor-like defect is neutral when being empty and becomes negatively charged when it traps an electron.

In our previous study, we have found the charge trapping effect in Al/SRO/Si MOS-like devices under vertical electrical stress [10]. The trapped charge can be either negative or positive, depending on the bias of the vertical stressing voltage. The trapped charge density depends on the thickness of the SRO layer, indicating that the charges are trapped not only at the SRO/Si interface region, but also in the bulk of the SRO layer. It is reasonable to assume that some donor-like and acceptor-like states are formed in SRO layer due to the excess Si. When applying a positive stressing voltage on the gate electrode, the energy band

Table 1. List of samples and their preparation parameters.

Sample	Structure	Ro for SRO	Thickness of SiO_2 (Å)
N1	Al/SRO/Al on Si	10	
N3	Al/SRO/Si on Si	20	
N2	Al/SRO/Si on Si	10	
N4	Al/SRO/Si on Si	20	
N7	Al/SRO/SiO_2/Al on Si	10	350
N9	Al/SRO/SiO_2/Al on Si	20	350
N8	Al/SRO/SiO_2/Al on Si	10	350
N10	Al/SRO/SiO_2/Al on Si	20	350

will bend downward and an electron accumulation layer is thus formed in the surface region of the n-type Si substrate. In this case, the acceptor-like defect states move below the Fermi level and they will capture negative charges; The SRO layer is thus negatively charged. On the other hand, if a negative bias is applied at the gate, an inversion layer will form in the surface region of the n-type substrate, the energy band will bend upward and the donor-like defect states move above the Fermi level. The donor-like defect states will lose their electrons and become positively charged and thus, the SRO layer will trap positive charges. It should be pointed out that, in both cases, the trapped charges in the SRO layer are due to the charge-exchange between the SRO layer and the Si substrate.

In the situation of lateral electrical stress, the stress voltage is applied coplanar. In order to understand the experimental results, we also measured the *C-V* curves of electrodes 1 and 2 respect to the substrate before and after lateral electric stress. It was found that the *C-V* curves of the positively biased electrode always shift to the right side, while the *C-V* curves of the negatively biased electrode always shift to the left side. That means that negative and positive charges were trapped in the SRO layer under the positively and negatively biased electrodes, respectively. That is an indication of the formation of an accumulation layer under the positively biased electrode and an inversion layer under the negatively biased electrode, respectively.

A model is proposed and schematically showed in Figure 1. Two channels for current to flow probably exist: one is through the SRO layer between the biased electrodes (electrode 1 and 2 in the figure); another channel is through the surface of the Si substrate. In the second channel, the current must flow through an accumulation layer below the positively biased electrode (electrode 1), an inversion and depletion layers below the negatively biased electrode (electrode 2), and a silicon surface layer between these two electrodes (from C to D in the figure). Most of the voltage should be dropped at the depletion layer and thus we can approximately consider that the potential of the Si surface between C and D is equal to that of the electrode 1 (because the applied voltage is very high, the voltage drop on the vertical SRO layer can be neglected). However, in the SRO layer, the potential is distributed linearly from A to B. Therefore, the average potential of the SRO layer below electrode 3 is lower than that of the Si surface under-layer. In this case, the energy band of this surface region should bend upward, as in the case of the gate electrode being negatively biased in the MOS-like structure. In this

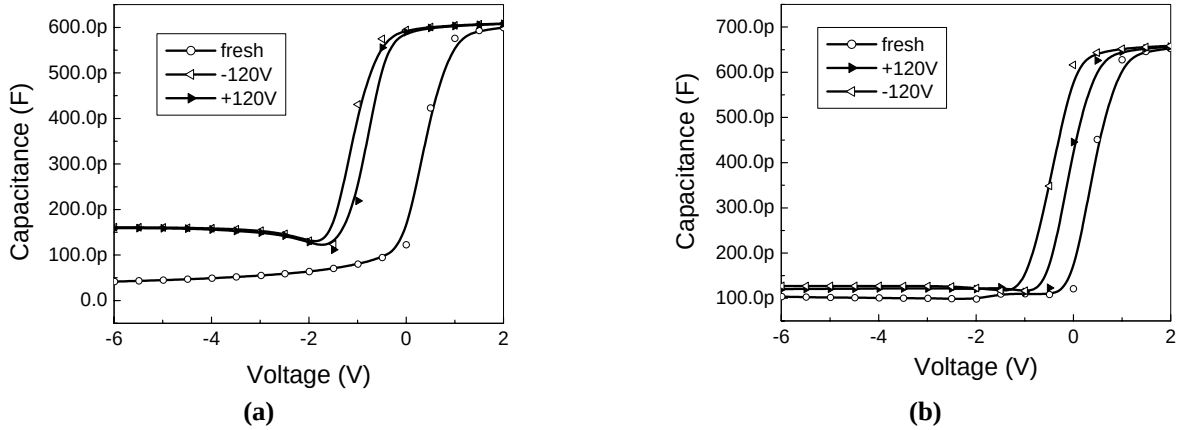
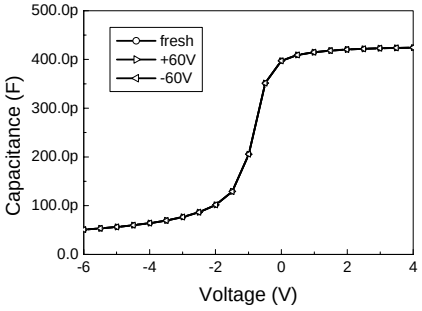


Figure 3: The CV curves of the annealed Al/SRO/Al on Si devices before and after lateral electrical stress. (a) Ro=10 and (b) Ro=20. The thermal annealing temperature is 1000°C/30min.



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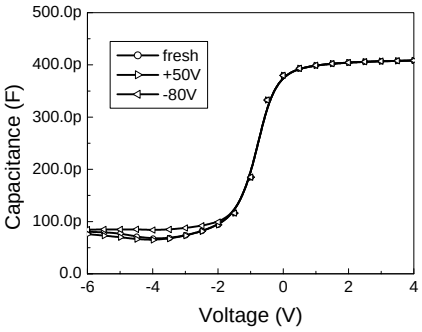
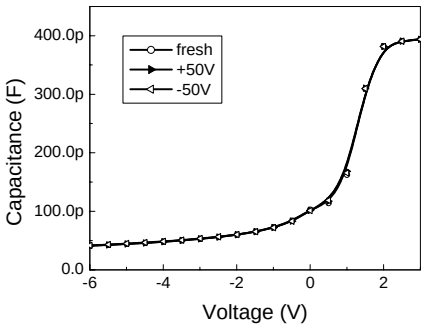


(b)

Figure 4: CV curves of as-deposited Al/SRO/SiO2/Al on Si devices before and after lateral electrical stress. (a) Ro=10 and (b) Ro=20.



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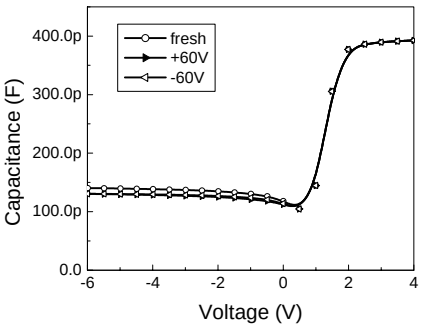

(b)

Figure 5: CV curves of annealed Al/SRO/SiO2/Al on Si devices before and after lateral electrical stress. (a) Ro=10 and (b) Ro=20. The thermal annealing temperature is 1000°C/30min.

case, positive charges will be trapped in region AB of the SRO layer. When measuring the C-V curves after the lateral stress, they should shift to the left due to the effect of trapped positive charges. Obviously, changing the bias of electrodes 1 and 2 can not change the type of trapped charges in the SRO layer; therefore, only positive charges can be obtained.

In the devices with structure Al/SRO/SiO_2/Al on Si, due to the blocking effect of the SiO_2 layer, the SRO layer and the Si surface can not exchange charges although the surface region of the Si substrate is still negatively biased.

The conductivity of the SRO layer depends on the Si excess and in a minor proportion on the thermal treatment. For the as-deposited SRO films, the excess Si atoms are uniformly distributed in the SRO layer; defect state is probably associated with each excess Si atom or cluster. However, higher Si excess makes the SRO films more conductive and electrons can move through the SRO layer easily. In this case, the trapped charges in the defect states can easily escape, thus it is difficult to obtain high density of trapped charges. Therefore, we observed smaller shift in the as-deposited single layer samples with Ro=10 compared to that of Ro=20. Similar results were obtained in the vertical electrical stress in our previous study [10].

The excess silicon in SRO acts in two different ways: as charge-trapping centers and as sites that provides conduction trajectories for carriers. After thermal annealing, the excess silicon atoms would segregate to form Si nanocrystals that results in the formation of stoichiometric SiO_2 phase with Si nano-crystals embedded [8]. Also it is expected that defect density reduces and the distance between the Si nanocrystals increases. Thus the electron transport by tunneling through these Si nanocrystals becomes difficult. In another word, it would be more difficult for the trapped charges at the Si nanocrystals to escape. That is why the trapped charge density increases after annealing for samples with Ro=10. For samples with Ro=20, due to the less excess Si concentration, the release of trapped charges is difficult even in the as-deposited state. However, thermal annealing will further lower the defect state density; thus, the trapped charge density will decrease after annealing. The effect of thermal annealing on the charge-trapping properties of SRO has been discussed in detail in reference [12].

5. Conclusion

A lateral charge trapping effect in SRO on Si devices was observed. The trapped charges are positive, with their density depending on the deposition and post thermal annealing conditions. Inserting an insulating SiO_2 layer between the SRO and Si will annihilate this lateral charge trapping effect because the charge exchange between SRO and Si substrate is not probable. The experimental results can be explained considering the potential modification in the surface of Si substrate, where an accumulation layer and an inversion layers will form respectively under the positive and negative biased electrodes.

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