Determination of recombination lifetime in MOS structures using a lineal voltage-sweep technique

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A lineal-voltage sweep technique for measurements of recombination lifetime in MOS structures is proposed. When a fast lineal – voltage ramp is applied to the gate of an MOS capacitor a non-equilibrium depletion layer is formed and electron-hole generation start in the space charge region and in the bulk. At elevated temperature the quasi-neutral region generation dominates rather than the space charge region generation. Then the diffusion length, and consequently the recombination lifetime, can be determined. Experimental results are shown.

Keywords: Recombination Lifetime; Lineal-Voltage Sweep; MOS Structures

1. Introduction

Lifetime measurements are of great importance for device and process characterization since these techniques are more sensitive to the impurities and other kinds of crystalline defects than the other methods based on the chemical or physical trace analysis [1]. No other method can detect defects as low as \(10^{10} - 10^{11}\) cm\(^{-3}\) in a simple room temperature measurement. In principle there is no limit to the defect density determined by lifetime measurement [2]. Various methods for the measurement of lifetime have been developed [3]. As it is known, there are two types of lifetime: recombination lifetime (\(\tau_r\)) and generation lifetime (\(\tau_g\)), but very often they are confused. The concept of recombination lifetime can be applied when excess carriers decay as a result of recombination. During recombination an electron – hole pair is annihilated at the average time \(\tau_r\). The generation lifetime, by analogy, is the average time that takes to generate an electron – hole pair. The other difference between them is that while the generation lifetime is measured in the space charge region (SCR), the recombination lifetime is measured in a distance determined by the diffusion length in the volume of the semiconductor. Because generation and recombination lifetimes are measured in different volumes of the material, it is very useful to measure both lifetimes on the same sample. The measurement of both parameters can provide useful information in device and process characterization. However, for the measurement of generation and recombination lifetime usually different techniques and different test structures are used.

Several techniques for measurement of recombination lifetime in MOS structures have been proposed [4-6]. However, they have not found wide acceptance because of experimental and data manipulation difficulties except the one proposed by Schroder et al. [6]. In that case, the same pulsed MOS capacitor technique as in the case of generation lifetime measurement is used but at elevated temperature, when the diffusion current dominates over the SCR generation current. This technique is very easy to implement. However, the weakness of the method is that the recombination lifetime (\(\tau_r\)) is proportional to \(1/4N_B^4\).

It is evident that any error in \(N_B\) (bulk concentration) will introduce a very large error in \(\tau_r\).

In this work, a simple method for measurement the recombination lifetime in MOS structures is proposed. The method is much less sensitive to the bulk doping concentration and it is easy to implement.

2. Theory

When a fast voltage ramp is applied on the gate of an MOS capacitor a non-equilibrium depletion layer arises. Different generation mechanisms attempt to re-establish the equilibrium. According to [2], the relation between the voltage sweep rate \((R = dV/dt)\) and the steady state generation in the SCR and in the bulk of an n-type semiconductor is:

\[
\frac{q\varepsilon_s \varepsilon_w \varepsilon_{ox} N_B}{C^3}\frac{dC}{dt} = \frac{q}{\tau_g} W + \frac{q n_i S_g A_g}{A_g} + \frac{q n_i S_g}{N_B L_p} - C \frac{R}{C_{ox}}
\]

(1)

where \(A_g = 2\pi r\), \(W\) is the area of the lateral SCR and \(A_g = \pi r^2\) is the gate area. After some transformations we can write eq. (1) as
Figure 1. C-V h.f characteristics for a MOS structure at 85 °C.

\[ C' \frac{dC}{dt} = \frac{1}{q\varepsilon Si\varepsilon S_D} \left[ \frac{C_{ox} C_f}{C} - C_{ox} C_f \right] + \frac{q n f S}{C_{ox} N_D L_p} - R \]

(2)

where \( C_{ox} \) is the oxide capacitance, \( C_f \) is the inversion capacitance, \( \tau_g \) is the effective generation lifetime

\[ \tau_g^* = \frac{\tau_g}{1 + 2S_0 \tau_g^*} \]

(3)

\( \tau_g \) is the generation lifetime, \( S_0 \) is the surface generation velocity under the gate, \( S_0 \) is the generation velocity of the lateral depleted surface, \( q \) is the charge of electron, \( n_i \) is the intrinsic concentration, \( N_D \) is the doping concentration, \( \varepsilon_{si} \) and \( \varepsilon_s \) are the silicon dielectric constant and the permittivity of the free space, respectively, \( L_p^* \) is the effective diffusion length [6] which characterizes the diffusion current in the quasi-neutral bulk as well as the surface generation velocity at the back surface of the sample. If the wafer thickness \( d >> L_p \), \( L_p \) is the diffusion length, then

\[ L_p^* = L_p \]

(4)

\[ L_p = \sqrt{D_p \tau_g} \]

(5)

The diffusion constant is given by

\[ D_p = \frac{kT}{q} \]

(6)

where the mobility of holes is given by [7]

\[ \mu_p = 495 \left( \frac{300}{T} \right)^{2.2} \]

(7)

The intrinsic carrier concentration can be calculated by the expression [8]

\[ n_i = 3.87 \times 10^{16} T^{1.5} \exp \left( \frac{0.605}{kT} \right) \]

(8)

Now, if a depleting linear voltage ramp of the form

\[ V(t) = V_0 + Rt \]

(9)

where \( V_0 \) is the offset voltage, is applied on the gate of a MOS capacitor, it goes into deep depletion. In this case, the depletion region width and the carrier generation in the SCR increase. When the generation rate becomes sufficiently large, so as to balance the rate of the charge being added to the gate, the capacitance reaches the saturation value \( C_{sat} \). The capacitance \( C_{sat} \) changes neither with the voltage nor with the time. Then at \( C = C_{sat} \), \( dC/dt = 0 \) in the left hand side of eq. (2). Neglecting the diffusion current, given by the third term in the right hand side of eq. (2) (for instance, at room temperature) a linear relation between \( R \) vs \( (C_f/C_{sat} - 1) \) is obtained. Getting a family of curves, varying \( R \), the effective generation lifetime can be obtained from the slope of the plot \( R \) versus \( (C_f/C_{sat} - 1) \) and from the interception of this curve with Y axis, \( S_g \) can be obtained [9].

However, at high temperatures, when the diffusion current (the third term in the brackets) is dominant, eq. (2) becomes;

\[ C' \frac{dC}{dt} = \frac{1}{q\varepsilon Si\varepsilon S_D} \left( \frac{q n_i^2 D_p}{C_{ox} N_D L_p} - R \right) \]

(10)

When the device enter in the saturation regime, \( C = C_{sat} \), i.e. \( dC/dt = 0 \), eq. (10) becomes

\[ R = \frac{q n_i^2 D_p}{C_{ox} N_D L_p} \]

(11)

Integrating eq. (11) from \( t = t_{sat1} \) to \( t_{sat} \) and from \( V_{sat1} \) to \( V_{sat} \), we find;


\[ 1 - \frac{V_{sat}}{V_{sat1}} = -K(t_{sat} - t_{sat1}) \]  \hspace{1cm} (12)

where

\[ K = \frac{qn_i^2 \sqrt{D_p}}{C_{ox} N_D V_{sat1} \sqrt{\tau_r}} \]  \hspace{1cm} (13)

\( V_{sat} \) is the saturation voltage, corresponding to \( C_{sat} \) and \( t_{sat} \) is the saturation time corresponding to the same point.

Changing the sweep rate of the applied voltage, we obtain a family of C–V curves. If the temperature is sufficiently high so that the diffusion current dominates the plot \( 1 - (V_{sat}/V_{sat1}) \) versus \( t_{sat} \) will be a straight line and from its slope, \( K \), we can determine

\[ \tau_r = \left( \frac{qn_i^2 \sqrt{D_p}}{C_{ox} N_D V_{sat1} K} \right)^2 \]  \hspace{1cm} (14)

If the experimental plot, \( 1 - (V_{sat}/V_{sat1}) \) versus \( t_{sat} \), is not linear the temperature must be raised until a straight line is obtained.

3. Experimental results

The samples were prepared on 2.5 to 5 ohm-cm phosphorous-doped silicon wafers. The oxidation was performed in dry \( O_2 + 2\% TCA \) (\( C_2H_3Cl_3 \)) ambient at 1000 °C. The oxide thickness, measured by an ellipsometer, was 800 Å. After the oxidation a 30 minutes thermal treatment in \( N_2 \) ambient at 1000°C was performed. The wafers were gotten by a backside P ion implantation with energy of \( E=120KeV \) and implantation dose of \( D=10^{14} \text{ cm}^{-2} \). The wafers were annealed at 900°C for 90 minutes. The oxide of the backside of the wafers was removed. Aluminum was evaporated on the both sides of the wafers and an annealing in \( N_2/H_2 \) ambient at \( T=430\degree \text{C} \) was performed. On the top of the wafers a dot electrodes were formed by lithography.

The lineal-voltage C-V measurements were performed with a Boonton 72 capacitance meter. A WAVETEK 175 waveform generator was used as a voltage source. The high frequency C-V and C-t measurements were performed with an MDC C-V system.

First of all, the standard high frequency C-V and C-t curves at room temperature were measured. The generation lifetime was found to be 173 \( \mu \text{s} \). After that, measurements at different temperatures were performed to found that at temperature of 85°C the diffusion component is dominant (the third term of eq.(2)). Then a family of C–V curves was obtained at that temperature. The voltage sweep rate was changed by a change of the voltage amplitude. The set of the experimental C-V curves is shown in Fig. 1. From these C–V curves, the \( I-V_{sat}/V_{sat1} \) versus \( t_{sat} \) plot was obtained, and is shown in Fig. 2. As can be seen the linearity is very good. From the line slope in figure 2 we obtained \( \tau_r = 3.6 \times 10^{-7} \text{ s} \). that corresponds to \( L_p = 1.93 \times 10^{-3} \text{ cm} \).

The value of the effective diffusion length is smaller than the wafer thickness (300 \( \mu \text{m} \)). That means, that it is the actual diffusion length related to the recombination lifetime by \( L_p = \sqrt{D \tau_r} \).

For comparison and confirmation of the method, the diffusion length from the 85°C C-t curve using the method of Schroder et al. [6] was determined. \( L_p = 1.54 \times 10^{-3} \text{ cm} \), was obtained using this method, which gives \( \tau_r = 2.29 \times 10^{-7} \text{ s} \)

The values of the diffusion length measured by the both methods are very close.

4. Conclusions

A recombination lifetime measuring method in MOS structure is presented. It allows generation and recombination lifetime to be measured in the same MOS structure. The measurements were performed at 85°C so that the diffusion current component dominates over SCR generation current. The method is simple and less sensitive to the bulk concentration compared with other methods. The results obtained by this method are very close to these obtained by the method of Schroder. In this experiment a ratio \( \tau_g/\tau_r = 480 \) was found. Usually the difference between the generation and recombination lifetime is approximately one order of magnitude. In the present case this ratio is relatively high. One can assume that the reason for this is that the neutral bulk of the semiconductor was cleaned by the metallic impurities during to the gettering process.

As a weakness of the method can be pointed out that a family of C-V curves must be obtained.

References