Superficies y Vacío ***17(2)***, *29-31, junio de 2004*

Determination of recombination lifetime in MOS structures using a lineal voltage-sweep technique

P. Peykov, M. Aceves
Instituto Nacional de Astrofísica, Óptica y Electrónica
Ap. Postal 51 y 216, 72000 Puebla, Pue., México

T. Diaz
Centro de Investigaciones en Dispositivos Semiconductores
Universidad Autónoma de Puebla
Av. Sn. Claudio y 14 sur S/N, Col. San Manuel, Puebla 72570, Puebla México
(Recibido: 15 de abril de 2002; Aceptado: 26 de mayo de 2004)

A lineal-voltage sweep technique for measurements of recombination lifetime in MOS structures is proposed. When a fast lineal – voltage ramp is applied to the gate of an MOS capacitor a non-equilibrium depletion layer is formed and electron-hole generation start in the space charge region and in the bulk. At elevated temperature the quasi-neutral region generation dominates rather than the space charge region generation. Then the diffusion length, and consequently the recombination lifetime, can be determined. Experimental results are shown.

Keywords: Recombination Lifetime; Lineal-Voltage Sweep; MOS Structures

1. Introduction

Lifetime measurements are of great importance for device and process characterization since these techniques are more sensitive to the impurities and other kinds of crystalline defects than the other methods based on the chemical or physical trace analysis [1]. No other method can detect defects as low as 10^{10} - 10^{11} cm^{-3} in a simple room temperature measurement. In principle there is no limit to the defect density determined by lifetime measurement [2]. Various methods for the measurement of lifetime have been developed [3]. As it is known, there are two types of lifetime: recombination lifetime (τ_r) and generation lifetime (τ_g), but very often they are confused. The concept of recombination lifetime can be applied when excess carriers decay as a result of recombination. During recombination an electron - hole pair is annihilated at the average time τ_r. The generation lifetime, by analogy, is the average time that takes to generate an electron – hole pair. The other difference between them is that while the generation lifetime is measured in the space charge region (SCR), the recombination lifetime is measured in a distance determined by the diffusion length in the volume of the semiconductor. Because generation and recombination lifetimes are measured in different volumes of the material, it is very useful to measure both lifetimes on the same sample. The measurement of both parameters can provide useful information in device and process characterization. However, for the measurement of generation and recombination lifetime usually different techniques and different test structures are used.

Several techniques for measurement of recombination lifetime in MOS structures have been proposed [4-6]. However, they have not found wide acceptance because of experimental and data manipulation difficulties except the one proposed by Schroder et al. [6]. In that case, the same pulsed MOS capacitor technique as in the case of generation lifetime measurement is used but at elevated temperature, when the diffusion current dominates over the SCR generation current. This technique is very easy to implement. However, the weakness of the method is that the recombination lifetime (τ_r) is proportional to $1/N_B^4$. It is evident that any error in N_B (bulk concentration) will introduce a very large error in τ_r.

In this work, a simple method for measurement the recombination lifetime in MOS structures is proposed. The method is much less sensitive to the bulk doping concentration and it is easy to implement.

2. Theory

When a fast voltage ramp is applied on the gate of an MOS capacitor a non-equilibrium depletion layer arises. Different generation mechanisms attempt to re-establish the equilibrium. According to [2], the relation between the voltage sweep rate ($R = dV/dt$) and the steady state generation in the SCR and in the bulk of an n-type semiconductor is;

$$\frac{q\varepsilon_0\varepsilon_s C_{ox} N_D}{C^3}\frac{dC}{dt} = \frac{qn_i^2}{\tau_g}W + \frac{qn_i S_0 A_s}{A_g} + qn_i S_g + \frac{qn_i^2 D_p}{N_D L_p^*} - C_{ox}R \qquad (1)$$

where $A_s = 2\pi r$, W is the area of the lateral SCR and $A_g = \pi r^2$ is the gate area. After some transformations we can write eq. (1) as

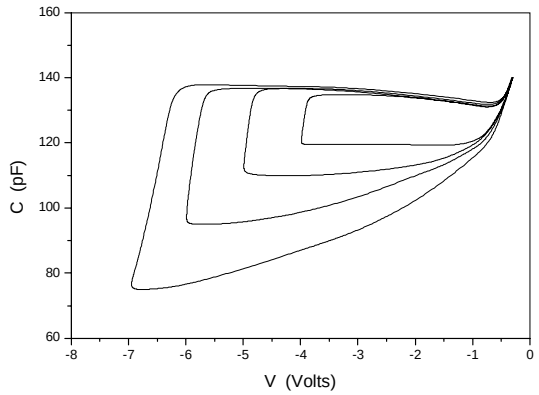

Figure 1. C-V h.f characteristics for a MOS structure at 85 °C.

$$C^{-3}\frac{dC}{dt}=\frac{1}{q\varepsilon_0\varepsilon_s N_D}\left[\frac{q\varepsilon_0\varepsilon_s n_i}{C_{ox}C_f\tau_g^*}\left(\frac{C_f}{C}-1\right)+\frac{qn_iS_g}{C_{ox}}+\frac{qn_i^2D_p}{C_{ox}N_DL_p^*}-R\right] \quad (2)$$

where C_{ox} is the oxide capacitance, C_f is the inversion capacitance, τ_g^* is the effective generation lifetime

$$\tau_g^*=\frac{\tau_g}{1+\frac{2S_0\tau_g}{r}} \quad (3)$$

τ_g is the generation lifetime, S_g is the surface generation velocity under the gate, S_0 is the generation velocity of the lateral depleted surface, q is the charge of electron, n_i is the intrinsic concentration, N_D is the doping concentration, ε_{si} and ε_o are the silicon dielectric constant and the permittivity of the free space, respectively, L^*_p is the effective diffusion length [6] which characterizes the diffusion current in the quasi-neutral bulk as well as the surface generation velocity at the back surface of the sample. If the wafer thickness $d >> L_p$, where L_p is the diffusion length, then

$$L_p^*=L_p \quad (4)$$

$$L_p=\sqrt{D_p\tau_r} \quad (5)$$

The diffusion constant is given by

$$D_p=\mu_p\frac{kT}{q} \quad (6)$$

where the mobility of holes is given by [7]

$$\mu_p=495\left(\frac{300}{T}\right)^{2.2} \quad (7)$$

The intrinsic carrier concentration can be calculated by the expression [8]

$$n_i=3.87x10^{16}T^{1.5}\exp\left(-\frac{0.605}{kT}\right) \quad (8)$$

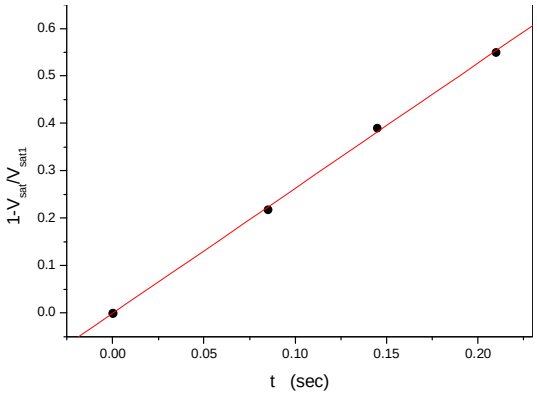

Figure 2. 1 - (V_{sat}/V_{sat1}) vs. t plot obtained form C-V curves from Fig. 1.

Now, if a depleting linear voltage ramp of the form

$$V(t)=V_0+Rt \quad (9)$$

where V_0 is the offset voltage, is applied on the gate of a MOS capacitor, it goes into deep depletion. In this case, the depletion region width and the carrier generation in the SCR increase. When the generation rate becomes sufficiently large, so as to balance the rate of the charge being added to the gate, the capacitance reaches the saturation value C_{sat}. The capacitance C_{sat}. changes neither with the voltage nor with the time. Then at $C = C_{sat}$. , $dC/dt=0$ in the left hand side of eq. (2). Neglecting the diffusion current, given by the third term in the right hand side of eq. (2) (for instance, at room temperature) a linear relation between R vs $(C_f/ C_{sat}. -1)$ is obtained. Getting a family of curves, varying R, the effective generation lifetime can be obtained from the slope of the plot R versus $(C_f/ C_{sat}. -1)$ and from the interception of this curve with Y axis, S_g can be obtained [9].

However, at high temperatures, when the diffusion current (the third term in the brackets) is dominant, eq. (2) becomes;

$$C^{-3}\frac{dC}{dt}=\frac{1}{q\varepsilon_0\varepsilon_s N_D}\left(\frac{qn_i^2D_p}{C_{ox}N_DL_p}-R\right) \quad (10)$$

When the device enter in the saturation regime, $C=C_{sat}$, i.e. $dC/dt=0$, eq. (10) becomes

$$R=\frac{qn_i^2D_p}{C_{ox}N_DL_p} \quad (11)$$

Integrating eq. (11) from $t=t_{sat1}$ to t_{sat} and from V_{sat1} to V_{sat}, we find;

$$1-\frac{V_{sat}}{V_{sat1}} = -K(t_{sat} - t_{sat1}) \qquad (12)$$

where

$$K = \frac{qn_i^2\sqrt{D_p}}{C_{ox}N_D V_{sat1}\sqrt{\tau_r}} \qquad (13)$$

V_{sat} is the saturation voltage, corresponding to C_{sat} and t_{sat} is the saturation time corresponding to the same point.

Changing the sweep rate of the applied voltage, we obtain a family of C–V curves. If the temperature is sufficiently high so that the diffusion current dominates the plot $1-(V_{sat}/V_{sat1})$ versus t_{sat} will be a straight line and from its slope, K, we can determine

$$\tau_r = \left(\frac{qn_i^2\sqrt{D_p}}{C_{ox}N_D V_{sat1}K}\right)^2 \qquad (14)$$

If the experimental plot, $1-(V_{sat}/V_{sat1})$ versus t_{sat}, is not lineal the temperature must be raised until a straight line is obtained.

3. Experimental results

The samples were prepared on 2.5 to 5 ohm-cm phosphorous-doped silicon wafers. The oxidation was performed in dry O_2*+2%TCA (*$C_2H_3CL_3$*)* ambient at 1000 °C. The oxide thickness, measured by an ellipsometer, was 800 Å. After the oxidation a 30 minutes thermal treatment in N_2 ambient at *1000°C* was performed. The wafers were gettered by a backside P ion implantation with energy of *E=120KeV* and implantation dose of $D=10^{16}cm^{-2}$. The wafers were annealed at 900°C for 90 minutes. The oxide of the backside of the wafers was removed. Aluminum was evaporated on the both sides of the wafers and an annealing in N_2/H_2 ambient at *T=430°C* was performed. On the top of the wafers a dot electrodes were formed by lithography.

The lineal-voltage C-V measurements were performed with a Boonton 72 capacitance meter. A WAVETEK 175 waveform generator was used as a voltage source. The high frequency C-V and C-t measurements were performed with an MDC C-V system.

First of all, the standard high frequency C-V and C-t curves at room temperature were measured. The generation lifetime was found to be 173 μs. After that, measurements at different temperatures were performed to found that at temperature of *85°C* the diffusion component is dominant (the third term of eq.(2)). Then a family of C–V curves was obtained at that temperature. The voltage sweep rate was changed by a change of the voltage amplitude. The set of the experimental C-V curves is shown in Fig. 1. From these C–V curves, the $1-(V_{sat}/V_{sat1})$ versus t_{sat} plot was obtained, and is shown in Fig. 2. As can be seen the linearity is very good. From the line slope in figure 2 we obtained $\tau_r = 3.6\ x10^{-7}\ s.$ that corresponds to $L_p=1.93\ x\ 10^{-3}\ cm$. The value of the effective diffusion length is smaller than the wafer thickness (300 μm). That means, that it is the actual diffusion length related to the recombination lifetime by $L_p = \sqrt{D_p\tau_r}$.

For comparison and confirmation of the method, the diffusion length from the 85°C C-t curve using the method of Schroder et al. [6] was determined. $L_p = 1.54\ x10^{-3}$ cm, was obtained using this method, which gives $\tau_r=2.29\ x\ 10^{-7}s$ The values of the diffusion length measured by the both methods are very close.

4. Conclusions

A recombination lifetime measuring method in MOS structure is presented. It allows generation and recombination lifetime to be measured in the same MOS structure. The measurements were performed at *85°C* so that the diffusion current component dominates over SCR generation current. The method is simple and less sensitive to the bulk concentration compared with other methods. The results obtained by this method are very close to these obtained by the method of Schroder. In this experiment a ratio $\tau_g/\tau_r=480$ was found. Usually the difference between the generation and recombination lifetime is approximately one order of magnitude. In the present case this ratio is relatively high. One can assume that the reason for this is that the neutral bulk of the semiconductor was cleaned by the metallic impurities during to the gettering process.
As a weakness of the method can be pointed out that a family of C-V curves must be obtained.

References

[1] D. De Busk and J. Van Wagoner, Semiconductor Int., **May**, 124 (1992).
[2] D. K. Schroder, Semiconductor Material and Device Characterization, 2º ed. (John Wiley & Sons, Inc., 1998)
[3] J. S Kang and D. K. Schroder, Phys. Stat. Solidi (a). **13,** 89 (1985).
[4] J. Muller and B. Schick, Solid State Electron. **13,** 1319 (1970).
[5] D. K. Schroder, IEEE Trans. Electron Dev. **ED-19,** 1018 (1972).
[6] D. K. Schroder, J. D. Whitfield and C. J. Varker, IEEE Trans. El. Dev. **ED-31,** 462 (1984).
[7] J. M. Dorkel and P. Lerturg, Sol. State El. **24,** 821 (1981).
[8] C. D. Thurmond, J. Electrochem. Soc. **122,** 100 (1976).
[9] R. F. Pierret, IEEE Trans. Electron Devices. **19,** 869 (1972).