New observation of single electron trapping effect in Si nanoclusters embedded in SRO layer

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I-V characteristics of Al/SRO/Si MOS devices were measured. Novel I-V curves, with extraordinary current peaks in both positive and negative bias, were observed. These current peaks are ascribed to the charging or discharging of the Si nanoclusters near the SRO/Si interface.

Keywords: Single-electron trapping; Si nanoclsuters; Silicon-rich oxide; Charging and discharging.

1. Introduction

Silicon Rich Oxide (SRO) has been extensively studied due to its special properties such as charge-trapping effect, strong light emitting, and variable carrier transport property depending on the excess silicon content. Some novel devices using SRO have been proposed based on these special properties [1-3].

SRO can be prepared by various techniques [4-6], such as Si implantation into thermal dioxide (SiO_2), plasma enhanced chemical vapor deposition (PECVD) and low pressure chemical vapor deposition (LPCVD). SRO deposited by LPCVD (LPCVD-SRO) is a two phase material, with excess Si nanoclusters (NCs) embedded in SiO_2 matrix [7]. In the LPCVD-SRO thin films, very obvious charge-trapping effect has been observed and the trapped charge density increases with decreasing the excess Si content [8]. Evidently, the trapped charges could be divided into two parts: the trapped charges in the bulk of SRO layer and those near the SRO/Si interface (in an Al/SRO/Si MOS device) [9]. The first one requires relatively high electrical field to be charged and discharged; while the later one can be injected from and released to the Si surface at relatively low electrical field. It is believed that [9] the charge-trapping centers are correlated with the embedded Si NCs in SRO. In this study, novel experimental observations in I-V characteristics of the Al/SRO/Si MOS devices are reported. A theoretical model is proposed based on the charge exchange between the SRO and Si substrate to explain the experimental results.

2. Experiments

Al/SRO/Si MOS devices were fabricated with SRO layer thickness from 20 to 360 nm. Both n and p-type (100) c-Si wafers with resistivity of 2-9 Ω-cm were used as substrate; the SRO layers were deposited by LPCVD using N_2O and SiH_4 as reactant gases and the gas flow ratio Ro= $[N_2O]/[SiH_4]$ =20. The excess Si content of the SRO layer is around 6.7% [6]. The front and back side contacts were achieved by Al evaporation. Front electrodes (gate electrode) with rectangular shape and area of 1.4×10^{-2} cm^2 were patterned by the standard photolithography technique. The samples were sintered at 450°C in forming gas for 20 minutes in order to get good contact.

I-V measurements were performed using a *HP precise semiconductor parameter analyzer 4145A*. The measurements were carried out at room temperature in the dark and inside a metal box to reduce the electric noise.

3. Results and discussion

Fig.1, 2 and 3 show the typical I-V curves for the samples with n-type substrates, and SRO thickness of 20, 90 and 360 nm, respectively. Similar I-V curves were observed for the samples with p-type substrate. From these figures, it can be observed:

a. All samples showed an upward current peak in the negative bias condition, whose position will change with the SRO thickness. This result agrees with that reported in [9].
b. Another current peak clearly observed in all samples is located in the positive bias side. Its position changes with SRO thickness. However, the observation of this peak strongly depends on the measurement parameters. It becomes clearer with fast voltage sweeping rate (the voltage sweeping rate was 3-4 V/S in this experiment). When the voltage sweeping rate is slow, the peak becomes smaller and even disappears. This current peak has very good reproducibility, which means that it always appears at similar voltage position during repeated measurements. Therefore, the possibility of noise can be eliminated and this peak is really due to

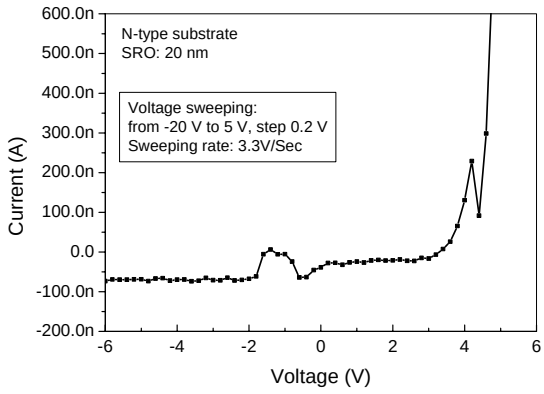

Figure 1. I-V curve of Al/SRO(20 nm)/Si device. Besides the current peak in the negative voltage side, another peak appears in the positive voltage side.

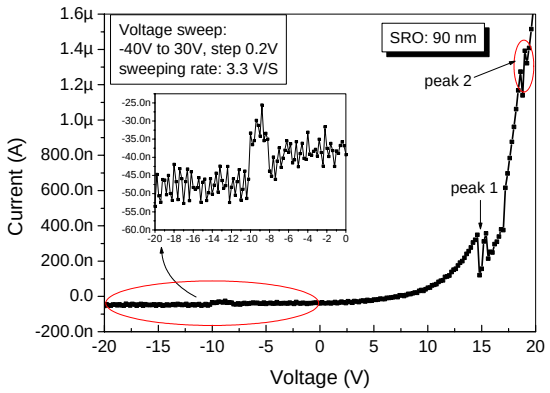

Figure 2. I-V curve of Al/SRO(90 nm)/ Si device. Besides the current peak in the negative voltage side, other two peaks appear in the positive voltage side.

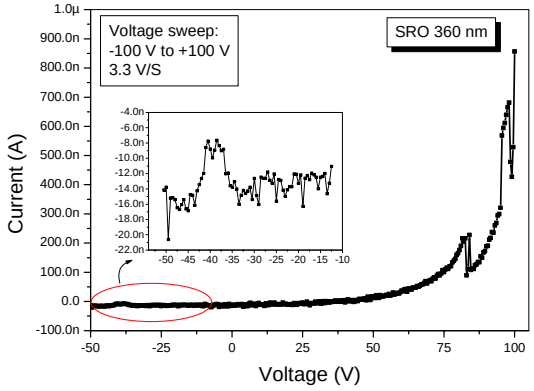

Figure 3. I-V curve of Al/SRO(300 nm)/ Si device. Besides the current peak in the negative voltage side, other two peaks appear in the positive voltage side.

some physical mechanisms of the devices.

c. A third current peak, which appears at a larger positive voltage, can be observed for samples with thicker SRO layer (90 nm and 360 nm).

As proposed previously [9], high density of interface-NCs exists in a thin layer near the SRO/Si interface. A very thin SiO_2 layer (thickness d_{INC}) separates the interface-NCs and the substrate. The band diagram is schematically shown in Fig.4. When the voltage is swept from negative to positive, the valence band (VB) of interface-NCs is well above the surface Fermi level in the beginning of the sweeping process. Then holes will be trapped in the VB of interface-NCs. However, during the voltage sweeping process the energy band of the interface-NCs will drop continuously. When the VB of interface-NCs drops down the surface Fermi level, it will release the trapped holes to the substrate, creating the upward current peak (Fig.4A). Obviously, this will happen at a negative bias. On the other hand, when the conduction band (CB) of interface-NCs drops across the surface Fermi level, electrons will be injected into the CB of the interface-NC. This electron injection process will cause an upward current peak at a positive voltage (Fig.4B).

The thickness of the SiO_2 layer, d_{INC}, has been estimated to be 2 nm based on the relationship between the current peak position and the SRO layer thickness, assuming that the valence band edge of the interface-NCs is aligned with that of the Si substrate [9]. In fact, the valence band edge of the interface-NCs should be somewhat below that of the Si substrate because of the band gap widening of the interface-NCs. Considering this effect, the value of d_{INC} will be larger than 2 nm. Assuming d_{INC}=4 nm, than we can estimate the energy difference (ΔE_c) between the conduction band edges of the interface-NCs and the Si substrate. Fig.5 shows the voltage drop on the SRO layer (V_{ox}) when the first current peak appears in the positive bias as function of SRO layer thickness (t_{ox}). A linear relation can be found:

$$V_{ox}=A+E_p\times t_{ox}=-3.47+0.22\times t_{ox}$$

Where E_p=0.22 V/nm is the electrical field in the SRO layer when the peak appears. Taking the surface potential as ψ_s=0.6 eV (which can be estimated according to the surface charge density), then the energy difference ΔE_c=1.35 eV (Due to the quantum confinement effect, the band gap of interface-NCs will be wider than that of Si substrate, and the CB of interface-NCs is above that of substrate. From Fig.4B, it is known that when the first current peak appears in positive bias, the CB of interface-NCs is aligned with surface Fermi level E_f. This happens due to the band bending of both Si surface and the SiO_2 sandwiched between interface-NCs and substrate. Thus $\Delta E_c+0.23=\psi s+ E_p\times t_{ox}$ and 0.23 eV is the energy difference between the Fermi level and the CB of the substrate. $E_p\times t_{ox}$ is the band bending of the sandwiched SiO_2 layer.) Because the current peak in the negative bias appears at electrical

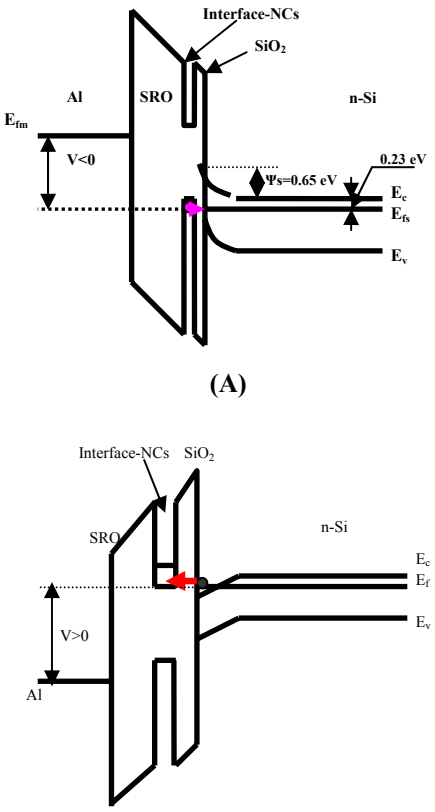

Figure 4. Band diagram of the Al/SRO/n-Si device under negative (A) and positive (B) bias, respectively.

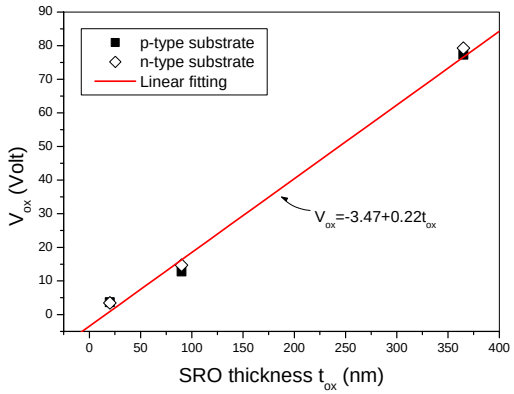

Figure 5. Voltage drop at SRO layer as function of SRO thickness when the first current peak in the positive voltage side appears. $V_{ox}=V_{peak}-0.6$ volt, where V_{peak} is the gate voltage at the first current peak in positive voltage side, and 0.6 volt is approximately the surface potential.

field of 0.118 V/nm [9], so the energy difference between the valence band edges of the Si substrate and the interface-NCs (ΔE_v) can be estimated similarly. ΔE_v=0.23 eV was obtained. Therefore, the band gap of the interface-NCs is 1.35+1.12+0.23=2.7 eV. Using the quantum model [10], the average diameter of the interface-NCs can thus be estimated to be about 15-20 Å. This is in agreement with the TEM results [11].

4. Conclusions

As a conclusion, I-V characteristics of the Al/SRO/Si MOS devices were observed in detail; current peaks appear in both negative and positive bias conditions. These new observation can be ascribed to the exchange of charges between the interface-NCs and the Si substrate, and is another evidence of the trapping charge effects in the Si NCs. From these observations it is possible to obtain the average diameter of the interface-NCs. The estimated average diameter of the interface-NCs is 15-20 Å, being in agreement with data already reported. The interface-NCs are separated by a SiO_2 layer from the substrate, and the SiO_2 layer may be formed unintentionally at the beginning of the LPCVD deposition process.

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